FIG. 1

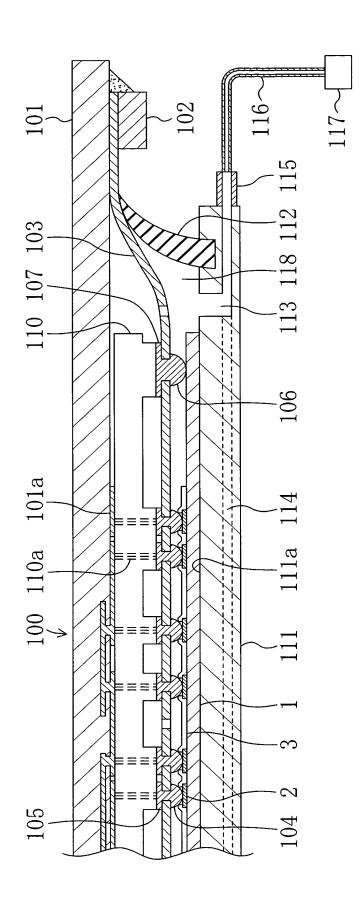
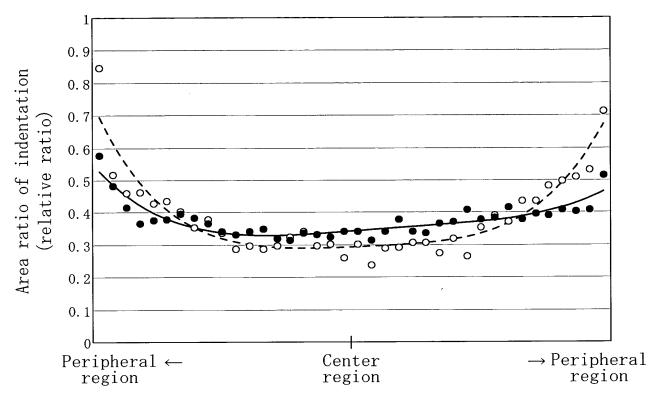


FIG. 2



Position in semiconductor wafer plane

FIG. 3A

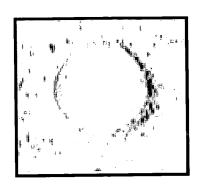


FIG. 3B

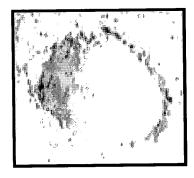


FIG. 3C

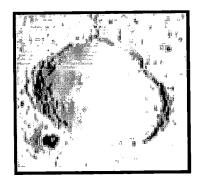


FIG. 4

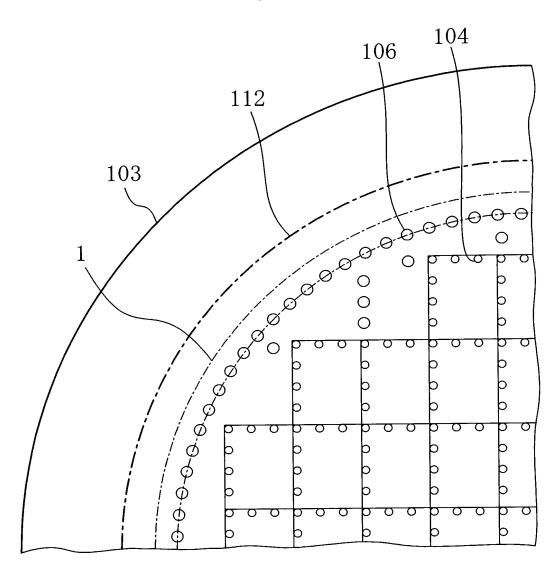


FIG. 5

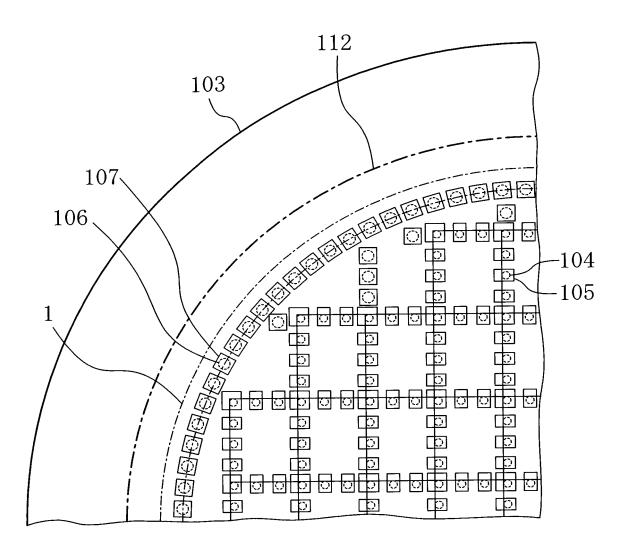
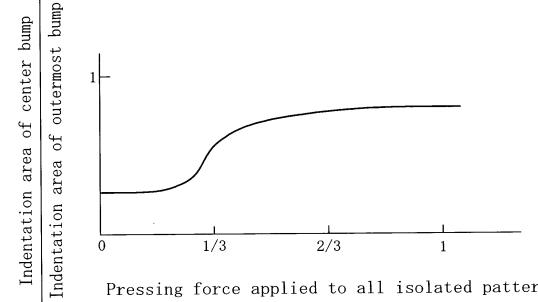


FIG. 6



Pressing force applied to all isolated patterns

Pressing force applied to all electrically connecting isolated patterns

FIG. 7
PRIOR ART

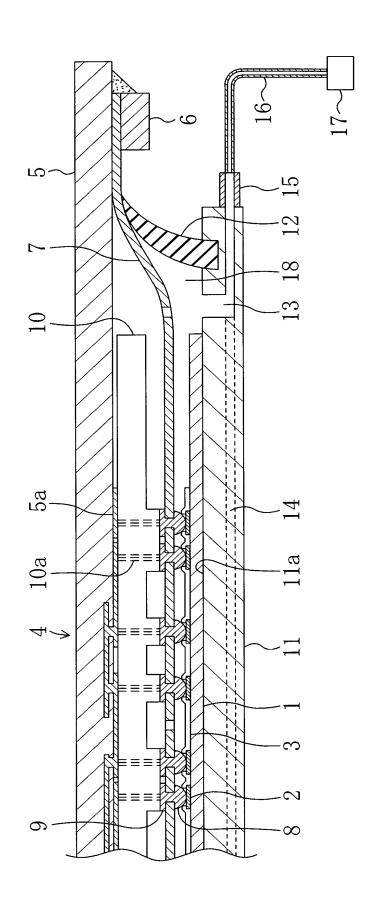
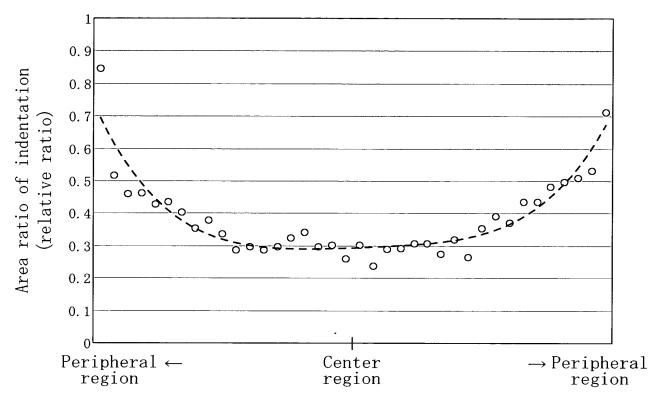


FIG. 8
PRIOR ART



Position in semiconductor wafer plane

FIG. 9A PRIOR ART

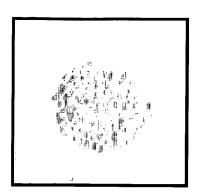


FIG. 9B PRIOR ART

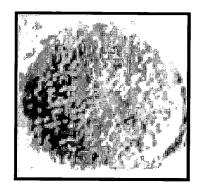


FIG. 9C PRIOR ART

